

DOCUMENTATION

INPUT - OUTPUT CARD

IO/2

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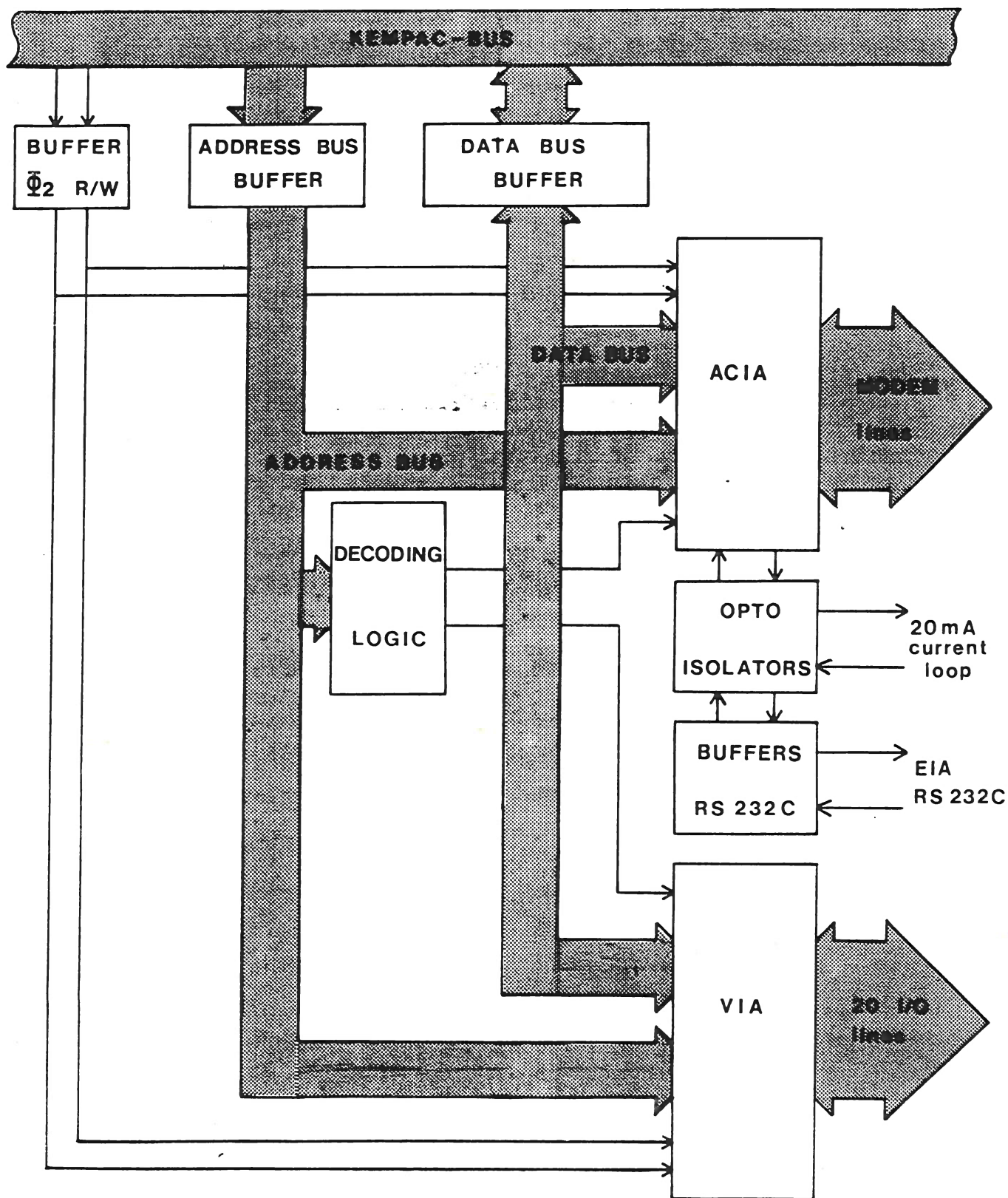
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1. FEATURES

- * 20 I/O lines with handshake capability and 2 16-bit timers
- * serial interface: RS 232C and current-loop
- * X-tal derived programmable baud rate generator
- * 15 possible baud rates from 50 to 19,200 baud
- * serial echo mode
- * false start bit detection
- * external 16x clock input for non-standard baud rates (up to 125 Kbaud)
- * programmable: word lengths, number of stop bits, and parity bit generation and detection
- * data set and modem control signals provided
- * parity : odd, even, none, mark, space
- * full-duplex or half-duplex operation
- * programmable 5, 6, 7, 8 and 9 bit transmission
- * serial input and output signals are optically isolated
- * buffered data, address and control lines
- * dip-switch selectable decoding in 32 bytes steps

2. BLOCK DIAGRAM



3. DESCRIPTION

The IO-2 card is designed to interface a KEMPAC system with a serial communication device, e.g. a CRT or TTY, in conformance with the specification of EIA Standard RS 232C or 20 mA current-loop. Opto-isolators are used to accomplish a electrical separation between the KEMPAC system and a serial device. Baud rate selection is possible under software control (50 -19,200 baud) and is derived from a standard 1.8432 MHz X-tal.

The 20 I/O lines may be used for connecting a parallel communication device or other user defined interfaces.

The card contains (see block diagram fig. 1):

- a. data address and control line buffers
- b. decoding logic
- c. a VIA (6522) for parallel I/O
- d. a ACIA (6551) for serial I/O with internal baud rate generator
- e. opto-isolators
- f. line driver and receiver

These circuits are described separately below.

a. Buffers

The data and address lines are buffered with the octal bus transceivers 74LS245 -IC 1, 2 and 3. The transceivers for the address lines however are used in a unidirectional mode (pin 1 is logic "1"). The signals O2 and R/W are buffered with a 74LS125 (a quad 3-state non inverting buffer).

b. Decoding logic

The IO-2 card occupies 32 bytes in the memory map. The lower 16 bytes are used by the VIA for its registers. The ACIA has 4 registers, therefore only the first 4 bytes of the second half are unique. To select a 32-bytes block in memory, the IO-2 card uses three 4-bit comparators (74LS85) - IC 6, 7 and 8. A comparison between the address lines A15 to A5 and 11 switches will decide whether the data bus transceiver will be enabled and the VIA/ACIA selected or not. An open switch will be regarded as a logic "1". Switch # 8 of the 8-pole dip-switch correspond with the address line A15; # 7 with A14 and so on. An example for selection from \$EC20 to \$EC3F is given below.

9
1001 1010 000

The address space in binary is : 1110 1100 001x xxxx

address	8-pole dip switch
A15=1	8 = open
A14=1	7 = open
A13=1	6 = open
A12=0	5 = closed
A11=1	4 = open
A10=1	3 = open
A9 =0	2 = closed
A8 =0	1 = closed
3 pole dip switch	
A7 =0	3 = closed
A6 =0	2 = closed
A5 =1	1 = open

This selection is to be preferred when the IO-2 card is used in a KEMPAC-SYSTEM 1, 2 or 3. This in relation with the available software.

c. The VIA

The VIA provides for 20 programmable I/O-lines; four of these lines can be used for handshake applications. Together with two 16-bit interval timers and a shift register a complex parallel I/O configuration can be realized. For further information on the 6522, refer to the data sheet (not included with the IO-2 description).

d. The ACIA

The 6551 is an Asynchronous Communication Adapter (ACIA) intended to provide for interfacing the 6500/6800 microprocessor families to serial communication data sets and modems. Further details are given in the data sheet of the 6551 (see appendix). When the input signals of the ACIA : DSR, DCD, RxC and CTS are not connected to an communication I/O-device, their logic level will be pulled up to logic '1' by R13..R16, when the four switches of S3 are open. Closing one of the switches will effect a logic '0' at the corresponding ACIA input. The dil switch S3 is specified according the following table:

S3 # 1	= DSR
S3 # 2	= DCD
S3 # 3	= RxC
S3 # 4	= CTS

A program example is given in chapter 4 for serial communication from a KEMPAC-SYSTEM to a CRT terminal (e.g. Hazeltine-1500)

e. Opto-isolators

The two opto-isolators (OC 1 and OC 2) separate the supply voltage of the IO-2 card from the connected serial in/output device up to a maximum of 2.5 kV. The straps J2, J3 and J4 should be present according to figure 2a. An external power supply of +12 V and -12 V, electrically separated from the KEMPAC-SYSTEM, has to be connected to the IO-2 header. If separation is not needed, the internal power supply may be used. The straps are now to be configured according to fig. 2b. This last configuration is factory installed.

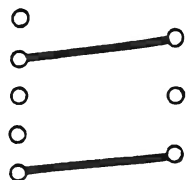


fig. 2a

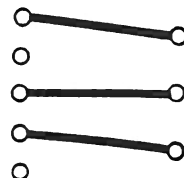


fig. 2b

f. Line driver and receiver

The line driver (75188) and receiver (75189), IC 9 and IC 10, interface data terminal equipment with data communication equipment in conformance with the specifications of EIA Standard RS 232C. The line driver has a limited output current of typical 10 mA. It is possible to reduce the standard output swing (± 12 V) to TTL levels by inserting the diodes D1 and D2 (1N4148 or equivalent).

The receiver has an input signal range of ± 30 V (absolute maximum) and a build-in hysteresis. A capacitor can be connected (see schematic drawing marked: *) from pin 12 to ground to provide input noise filtering.

4. PROGRAM EXAMPLE

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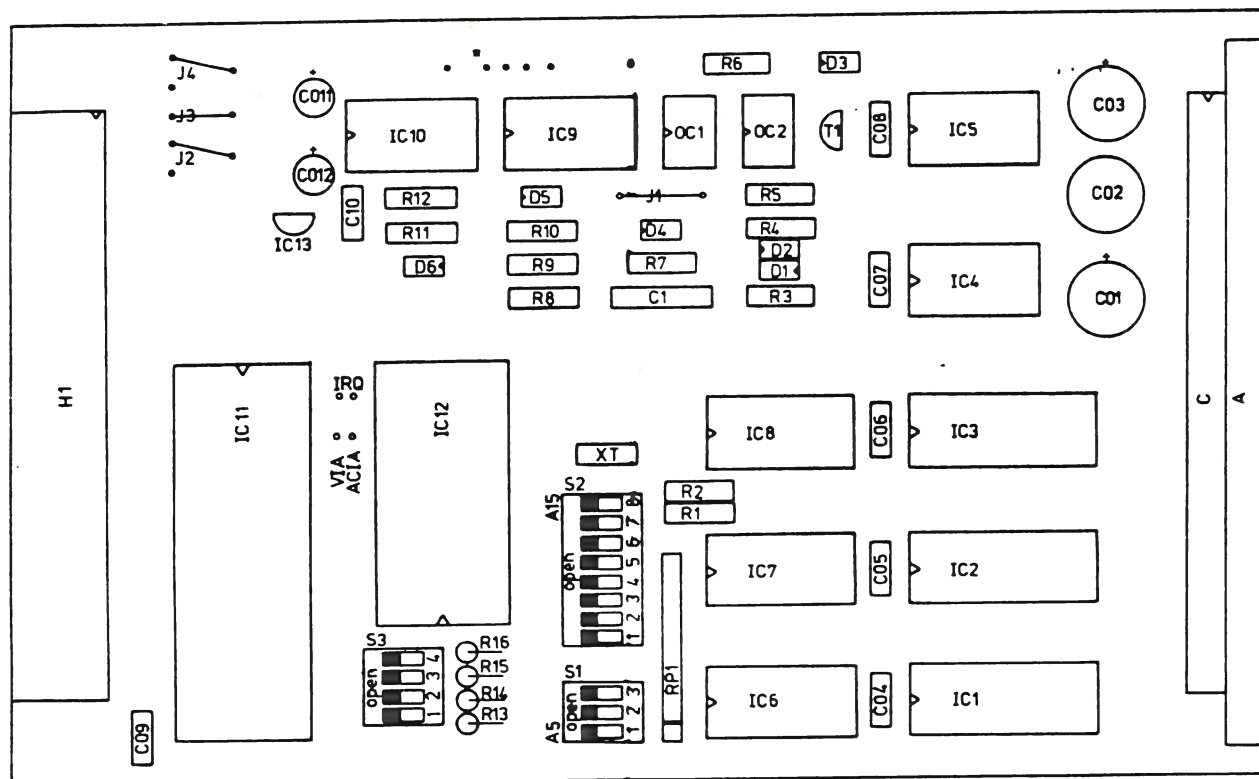
0010 ;TEST PROGRAM FOR KEMPAC I/O-2 CARD
0020 ;Version 1.0
0030 ;Date 15-9-1982
0040 ;
0050 ;Switches 2 and 4 of DIL-switch S3 must be closed.
0060 ;Connect "transmitted data" to "received data"
0070 ;(I/O header pin 17 and pin 20)
0080 ;
0090 ;
0100         .LS
0110         .DS
0120         .BA $A000
0130 ;
0140 ;LABEL DEFINITIONS
0150 INPUT   .DE $200
0160 OUTPUT  .DE $203
0170 INSVEC  .DE $206
0180 TDR     .DE $EC30
0190 RDR     .DE $EC30
0200 STATUS  .DE $EC31
0210 COMMAND .DE $EC32
0220 CONTROL .DE $EC33
0230 MONITOR .DE $F003
0240 ;
A000- D8     0250 ACIA   CLD
A001- 18     0260       CLC
A002- A9 00  0270       LDA #0
A004- 69 00  0280       ADC #%00000000 ;no parity
A006- 69 00  0290       ADC #%00000000 ;no echo
A008- 69 08  0300       ADC #%00001000 ;RTS low & TI disabled
A00A- 69 00  0310       ADC #%00000000 ;RI enabled
A00C- 69 01  0320       ADC #%00000001 ;DTR low
A00E- 8D 32 EC 0330       STA COMMAND ;store COMMAND-register
A011- A9 00  0340       LDA #0
A013- 69 00  0350       ADC #%00000000 ;1 stop bit
A015- 69 00  0360       ADC #%00000000 ;8 bits data
A017- 69 10  0370       ADC #%00010000 ;internal baudrate gen.
A019- 69 0F  0380       ADC #%00001111 ;19,200 baud
A01B- 8D 33 EC 0390       STA CONTROL ;store CONTROL-register
A01E- A0 00  0400 INITY  LDY #0
A020- B9 52 A0 0410 TESTLP LDA TEXT,Y
A023- F0 F9  0420       BEQ INITY ;last character
A025- C8     0430       INY ;next character
A026- 8D 30 EC 0440       STA TDR ;store TRANSMIT-register
A029- 20 06 02 0450 TESTLP1 JSR INSVEC ;look for ESCAPE
A02C- 90 03  0460       BCC TESTLP2 ;no ESCAPE
A02E- 4C 03 F0 0470       JMP MONITOR

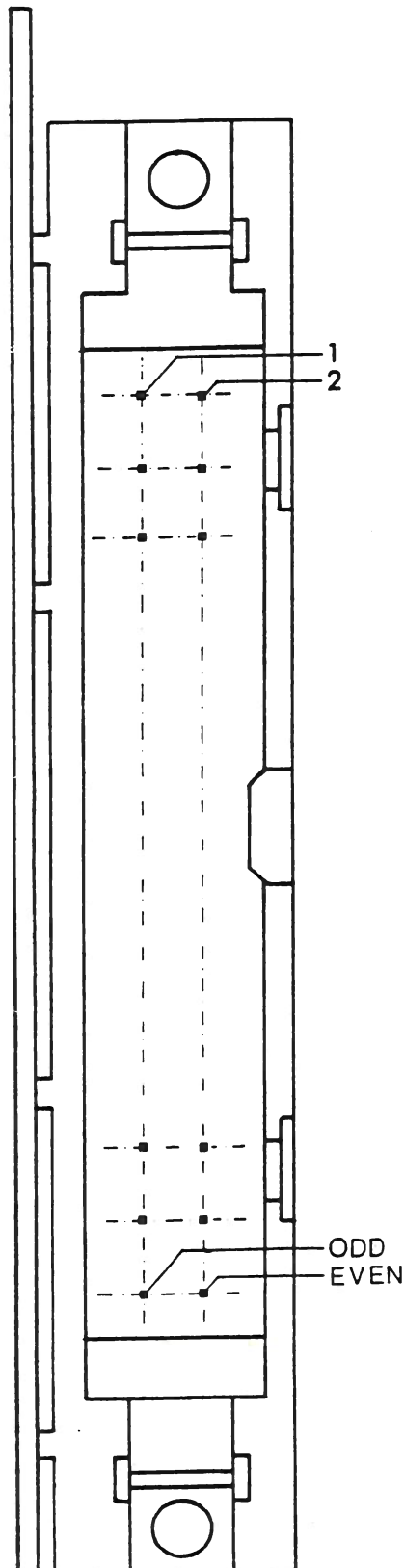
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5. REMARKS

When the signal RxD is used at the header pin 6, Jumper J1 must be removed, otherwise two outputs are tied together.

BOARD LAY-OUT.





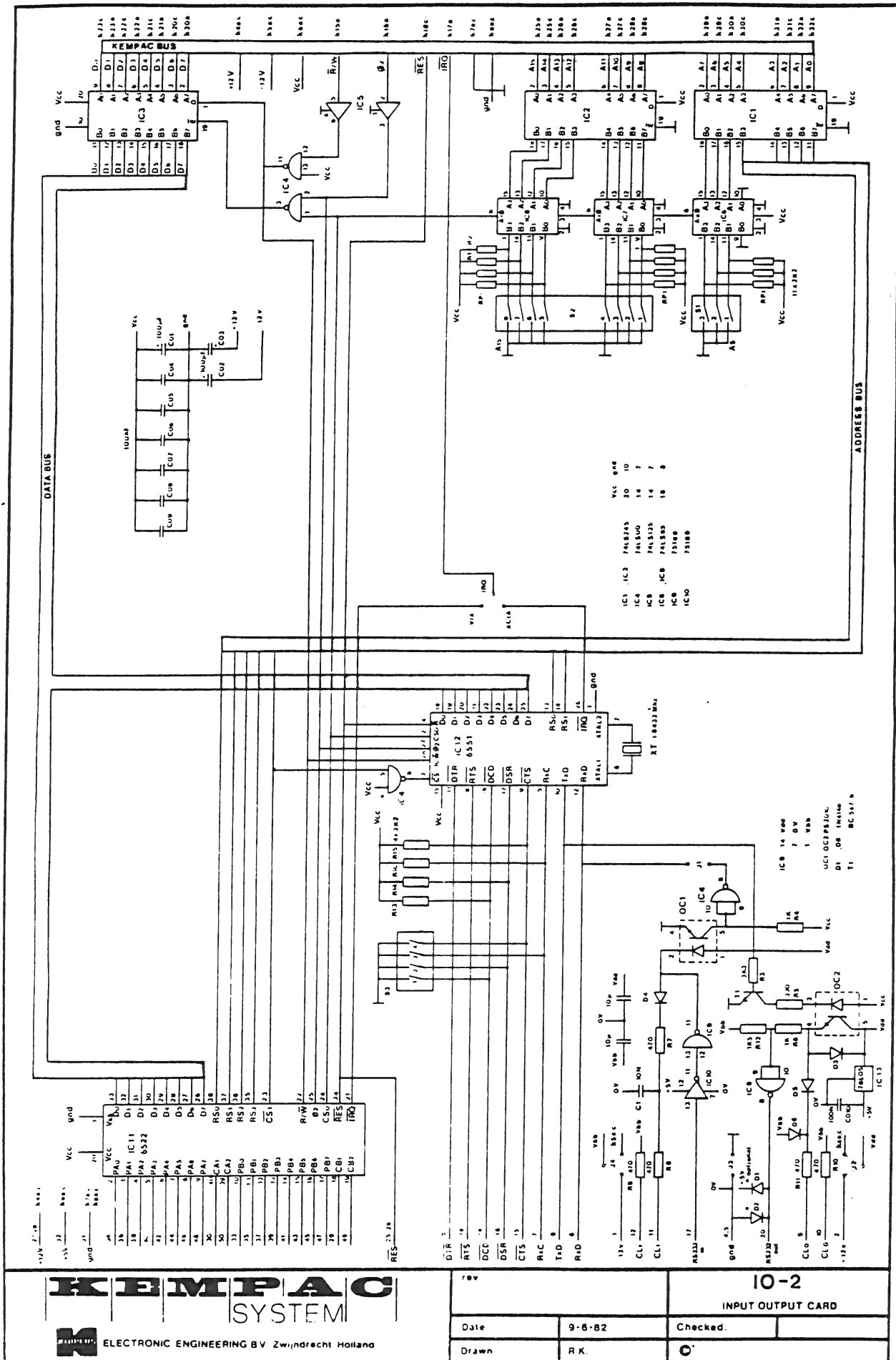
PIN	FUNCT.	DESCR.	PIN	FUNCT.	DESCR.
1	-12V		2	+12V	
3	gnd		4	gnd	
5	$\overline{\text{DTR}}$		6	RxD	
7	RxC		8	TxD	
9	printer out +	TTY	10	printer out -	TTY
11	keyboard in +	TTY	12	keyboard in	TTY
13	gnd		14	$\overline{\text{DCD}}$	
15	$\overline{\text{CTS}}$		16	$\overline{\text{DSR}}$	
17	received data	RS232C	18	$\overline{\text{RTS}}$	
19	n.c.		20	transm. data	RS232C
21	n.c.		22	n.c.	
23	n.c.		24	n.c.	
25	$\overline{\text{RESET}}$		26	RESET	
27	+12V		28	+12V	
29	CB1		30	CA1	
31	gnd		32	+5V	
33	PB0		34	PA0	
35	PB1		36	PA1	
37	PB2		38	PA2	
39	PB3		40	PA3	
41	PB4		42	PA4	
43	PB5		44	PA5	
45	PB6		46	PA6	
47	PB7		48	PA7	
49	CB2		50	CA2	

STROKE
[]

data taken

int/ext powersupply is strap selectable.

NOTE: A special flatcable is available for connecting



PIN	A	C
1	~A	~A
2	~B	~B
3	PWRFAIL	+5V BAT
4	+12V	+12V
5	-12V	-12V
6	+5V (Vcc)	+5V (Vcc)
7	GND	GND
8	GND	GND
9	P0	P1
10	P2	P3
11	P4	P5
12	P6	P7
13	CRT CONTROL	SYNC
14		
15	R/ $\bar{W}$	RDY
16	$\emptyset 2$	$\emptyset 1$
17	IRQ-REQ	IRQ-ACK
18	NMI	RESET OUT
19		
20	D7	D6
21	D5	D4
22	D3	D2
23	D1	D0
24	RESET IN	S.O.
25	A15	A14
26	A13	A12
27	A11	A10
28	A9	A8
29	A7	A6
30	A5	A4
31	A3	A2
32	A1	A0